THE THD PERFORMANCE OF SINGLE PHASE FIVE LEVEL INVERTER USING PR AND HARMONIC COMPENSATORS CURRENT CONTROLLER

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ABSTRACT

In order to meet the requirement from the industries demand aimed at a free-harmonics and high power rating source is remarkably increased in past few years. As compared to singlelev el inverter, multilevel inverter offers minimum harmonic distortion and higher power output. This project is to observe the THD performance of single phase five level inverter using proportional resonant (PR) and harmonic compensators current controller. The PR controller not only solve the current and harmonic problem, but also efficiency and accuracy of equipment in other application. The THD was reduced to 1.6% which is in the scope of the project. More functions were added to the PR current controller to reduce the THD at the 3^{th}, 5^{th}, and 7^{th}, harmonic orders. The THD of the 3^{th}, harmonic order was reduced from 0.45% to 0.1% while the, 5^{th}, and 7^{th}, harmonic orders were reduced from 0.6% and 0.43% to 0.25% and 0.4% respectively. The development and simulation is performed using Matlab/Simulink. The simulation result of experiment is performed by using Fast Fourier Transform analysis (FFT) for the harmonics captured.

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LIST OF SYMBOLS AND ABBREVIATION

AC	-Alternative Current
CHB_MLI	-Cascaded H-Bridge Multilevel Inverter
CMLI	-Cascaded Multilevel Inverter
DC	-Direct Current
f_{sw}	- Switching Frequency
I	- Current
IGBT	-Insulated-Gate Bipolar Transistor
MLI	-Multilevel Inverter
PWM	- Pulse Width Modulation
SPWM	-Sinusoidal Pulse Width Modulation
THD	-Total Harmonic Distortion
UTHM	-Universiti Tun Hussein Onn Malaysia
V	- Voltage

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CHAPTER 1

INTRODUCTION

1.1 Background Study

Cascade multilevel inverter (CMLI) structure has been attracting increasing interests in high power and medium voltage applications owing to its lower harmonics, high er efficiency and lower voltage stress compared to two or three level inverters [1][4]. Diode clamped, flying capacitors, and cascaded H bridge inverters (CHBI) constit ute several multilevel converter topologies presently in use. A cascaded multilevel i nverter consists of a serie of H bridge inverters with each H bridge unit having its own DC source or a single DC source and capacitors based DC sources for all but the first source. A cascaded multilevel inverter with k number of DC sources or nu mber of H bridge cells will provide (2k + 1) levels to synthesize the AC output wa veform. This means that for a five level inverte (FLI), two DC sources and two cas caded H -bridge cells are required [5][10].

Where a multicarrier PWM technique is adopted for obtaining the cascade in verter switching signals, n−1 carriers with same carrier frequency fc, and same peak to peak amplitude AC, are also required. For the five level cascaded inverter in for instance, the additional Hbridge inverter, DC source, and increase in the number of

carriers all add to increase in components count and costs that will ultimately lead to increase in switching losses and system size. Several attempts have been made in the recent past by researchers to synthesize the multilevel inverter (MLI) with few numb er of H bridge cells, circumventing the (2k + 1) levels hypothesis Even when high le vel MLI is to be developed from few number of H bridge cells, a quite number of au xiliary switches and diodes are usually incorporated in the power circuit resulting in additional control circuit designs for the switches in [11] for instance, where two H b ridge cells were deployed for an eleven level cascaded H bridge MLI, additional four switches and eight diodes were incorporated to realize the design objectives. In the p aper, no attempt was made to present the control circuit and its process of design whi ch is predicted to be complex. Inall the FLIs developed using a single H bridge cell [12], there are the presence of one or more auxiliary switches and diodes with additio nal control circuits. For instance, in some schemes two auxiliary switches with two a nti bidirectional diodes, two other diodes through which thecapacitors are discharged and two DC voltage sources have been deployed in addition to the single k cell struct ure [10], [16]. In other schemes, one auxiliary switch, four diodes and either two DC sources or two capacitors across a boost converter have in addition to the single k ce ll been designed to realize the FLIs output voltages[12],[14]. Due to the complexity o f the control circuit structures for the five level inverters, few authors presented the c ontrol scheme while many others made little orno attempt to discuss the processes of the control circuit designs.

1.2 Problem Statement

One of the important components in the system is the inverter which converts the DC energy stored in the battery banks to AC energy which will then use by consu mer or connected to power grid. As the current trend required cleaner power sourc e, higher output power, less losses and almost free harmonics, people are looking f orward for better inverter. Thus, a conventional single level inverter is no more rel evant to cope with the current trend. Nowadays, industries, researches are focusing to come out with inverter that can overcome the above mentioned issues. As a result, a multilevel inverter is created and first published by Nabae in 1980s to be able to generate output voltage and draw output current at very law distortion. The harmoni cs generated by Distributed

Power Generation Systems is also a major power quality issue, especially due to the fact that the number of these systems connected to the grid is always increasing. This means that it is very important to control the harmonics generated by these inverters to limit their adverse effects on the grid power quality. The current controller can have a significant effect on the quality of the current supplied to the grid by the inverter,and therefore it is important that the controller provides a high quality sinusoidal output with minimal distortion to avoid creating harmonics. A commonly used current controller for Single phase Inverters is the PR current controller. This controller is highly suited to operate with sinusoidal references like the reference used in Single phase Inverters, thus making it an optimal solution for this problem.

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1.3 Objectives

Based on the problem statements, there are three objectives that are going to be achieved. The objectives of this project are:

1. To model and simulate single phase five-level inverter to produce higher output power and less losses using Matlab/Simulink.
2. To investigate the THD performance of single phase five level inverter using PR current controller.
3. To reduce the 3^{th}, 5^{th}, and 7^{th} harmonics using harmonic compensator in PR current controller.

1.4 Scope of Study

The scope of this project is focused on to observe the current THD performance of single phase five level inverter using PR and harmonic compensators current controller designed. The power of this design will be 12kW while the voltage will be 400V. The THD will also be reduced to less than 5%. The design will focus to reduce the 3^{th}, 5^{th}, and 7^{th} harmonics. The designed single phase five level inverter with PR and harmonic compensator current controller will be simulated using Matlab/Simulink.

1.5 Report Structure

Chapter 2 will cover a theoretical frame work developed to provide a review about the topic, focusing in the selected papers which concentrate on Multilevel Inverters and reducing the THD. Chapter 3 will cover the outlined of research methodology. It will also discuss the measurement of the work as well as different aspects of the design. Chapter 4 will cover the result and discussion of the design. Finally, Chapter 5 will cover the conclusion of the project.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Multilevel inverters are used to get high voltages with low value of Total harmoni Di stortion (THD). For high power applications these are very much used. High worth of voltages can be gotten from a single DC source also. For the residual sources capacit ors can be used. Input voltage can be gotten from renewable foundations lik solar, wi nd also fuel cell. Multilevel inverters crop a step like waveform. When the amount of levels is augmented, the output waveform closely looks like sinusoidal waveform an d automatically THD value is reduced. Increased THD value makes several needless effects like heating, shaking, uneven changes in speed in the motors which are conne cted at the output of inverters. So, it is compulsory to use inverter which must be free from harmonics. So that today multilevel inverters are in high request for various ap plications. By dispersal proper control approaches also disadvantaged of addition any external mechanisms the required, harmonic free output waveform is following from multilevel inverters [1]-[2].

One switch in the obtainable topology is operated at low swapping occurrence which in turn reduces the switching stress and switching fatalities. The only drawback

is the upcoming topology uses a greater number of inductors and capacitors which may upsurge the size of the outline. Balamurugan et al [1] discussed about dissimil ar modulation methods including dissimilar references like sinusoidal, third harmon ic injection (THI), 60 degree and walked wave which are suitable for H Bridge M LI. Hasan et al [2], planned a new topology of a three phase half bridge multilevel inverter which includes two dissimilar structures.

The new simulation consequences were likened. Balamurugan et al [3] practic al space Based Three Phase Five Level H Bridge Inverter and inspected the results fo r dissimilar Inverted Sine Carrier PWM Strategies. Prabaharan and Palanisamy [4] co mplete a contrast of symmetric and asymmetric multilevel inverter which employs abr idged no of switches. balamurugan et al made an examination of various Unipolar In verted Sine Carrier Pulse Width Modulation techniques for the three faze Cascaded Multi Level Inverter and connected the results. Abraham and Benny [6] proposed a n ew topology of three phase seven level hybrid inverter which consists of three levels cascaded H Bridge and neutral point fastened multilevel inverter. Vinod Kumar et al [7] practical a single phase five level inverter and compared the results of multicarrier PWM technique with low swapping frequency PWM. Sambath et al [8] evaluated th e performance of dissimilar Multi Carrier PWM Approaches for a Single Phase Five Level H Bridge Type flying capacitor MLI. A. Shanmuga priyaa et al analyzed the pr esentation of Cascaded Z Source Multilevel Inverter which employs Third Harmonic Injection PWM technique. Wells et al [10] proposed a new modulation method which removes harmonics deprived of solving any mystical equations.

2.2 Review on the Relationship between the THD Level and Power Losses

In all, the realizations of the five level inverters were all power circuit based. The de sired levels of harmonics reduction informed the different choices of the control circu it designs by the authors. It is quite anticipated that if the realization of the FLI is co ntrol circuit based utilizing the single H bridge cell without auxiliary power compone nts rather than power circuit based utilizing the single H bridge cell with additional p ower circuit components, the resulting inverter will be smaller, lighter, and

simpler, implying greater reliability, lower cost and power conservation. Now a days, energy demand is rapidly increasing worldwide and poses a great challenge to all cou ntries for meeting the demand without significant impacts to the environment.

To meet the future energy demand, fossil fuels endure to be rummageisale a the primary energy source and therefore donate to the upsurge in greenhouse gases emission. But,Ithe impact could be lessened by incorporating renewable sources of e nergy such as solar and wind into the power system since they are clean also abund ant [1][3]. However, the energy source is sporadic in nature which requires advance d control especially in controlling it's power, now the photovoltaic (PV) system has a vital role in power generation, especially in distributed networks, due to easy add ition as well as being technologically proven [6][8]. Therefore, advance improveme nt of power converters especially for PV system is important to ensure efficient disp atch of PV power. The quality of power produced should be in compliance through international values such as IEC 61000.3.2 or IEEE 519 in the case of current harm onics responsibility. Inverters producing a sinusoidal output voltage and current thro ugh very low total harmonic distortion (THD) are important to achieve very high sy stem performance, efficiency, dependability, also stability. The attendance of harmo nics only leads to extra power losses, power quality decays, components breakdown , and reduced equipment lifetime.

2.3 Review on Power Circuit Diagram for the Inverter

The converters have to be designed to obtain a quality output voltage or a current wa veform with a minimum amount of ripple content. In high power and high voltage ap plications the conventional two level inverters, however, have some limitations in ope rating at high frequency mainly due to switching losses and constraints of the power device ratings. Numerous industrial applications have begun to require high power ap paratus in recent years. For the control of electric power or power conditioning the co nversion of electrical power from one form to another is necessary and the switching characteristics of the power devices permits these conversions. Inverters are the devic es that are used for conversion of DC to AC.

The output voltage of an inverter can be fixed type or variable type at fixed or variable frequency. A variable output voltage can be obtained by varying the input d c voltage andmaintaining the gain of the inverter constant. On the other hand, ifthe dc voltage is fixed variable output voltage can be obtained by varying the gain of the in verter. Inverter gain is defined as the ratio of ac output voltage to dc inputvoltage. In the conventional two level inverters the input DC is converted into the AC supply of desired frequency and voltage with the aid of semiconductor power switches. Depend ing on the configuration, four or six switches are used. A group of switches provide t he positive half cycle at the output which is called as positive group switches and the other group which supplies the negative half cycle is called negative group [18].

The proposed inverter by [18], uses minimum number of switches and less nu mber of voltage sources. The inverter circuit is shown in figure 2.1.The non compuls ory multilevel inverter topology has a single DC source and a single switch for makin gfive level outputvoltage. Residual four changes are provisional as schism altering un it.Since the upcoming circuit uses fewer no of bases then changes, the overall cost an d burden of the system is reduced. It is easy to crop compulsory no of gate signs whe n the no of switches are condensed. The obtainable inverter topology usages the switc hes S1, S2, S3, S4 and S5, S1 is rummage sale for creating five levels and switches S2 to S5 is used as a polarity changing unit.

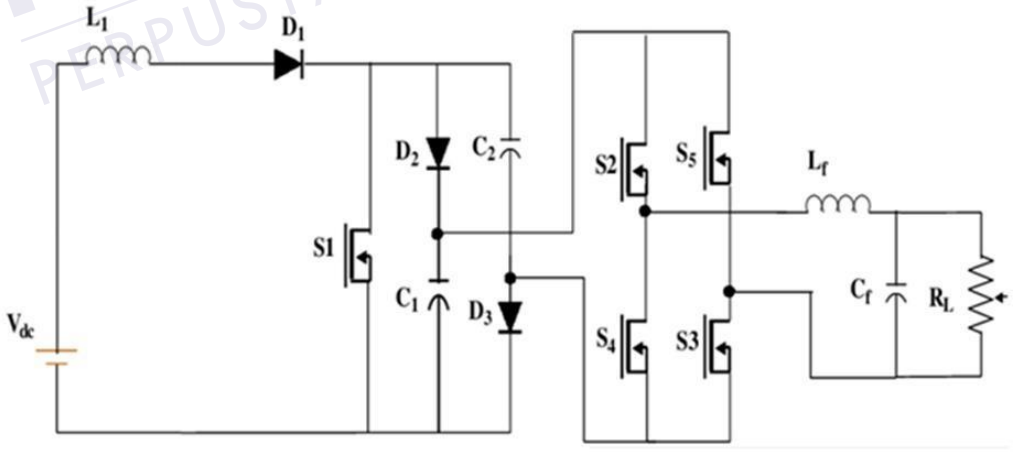


Figure 2. 1: Power circuit diagram of proposed inverter [18].

L1 is the increasing inductor which is used to boost the input voltage. The boost ed inputvoltage is given as input to the rest of the unit of inverter. Two diode capacitor legs are used in the power circuit diagram. The upcoming circuit uses a single source of less value than the rest of the sources are replaced by capacitors. Lf and Cf are the filt er mechanisms [18].

2.3.1 Review on Single-Phase Five-Level Inverter

The single phase five level inverter discussed here is a two stage circuit. Its fore stag e is a multilevel DC converter consisting of voltage source, switch tube, diode, and c apacitance; its backward stage is H Bridge. C1, C2 DC side split capacitance; Vc1, Vc2 DC side split capacitor voltage; Q1, Q2 capacitance C1, C2 charge discharge co ntrol switch; SCascade multilevel inverter (CMLI) structure has been attracting cumul ative benefits in high power and medium voltage requests owing to its lower harmoni cs, higher efficiency and lower voltage stress associated to two or three level inverte rs Diode clamped, flying capacitors, also cascaded H bridge inverters (CHBI) found s everal multilevel converter topologies presently in use. A cascaded multilevel inverter covers of a series of H bridge inverters through each H bridge unit having its own D C source or a single DC source and capacitors based DC sources [3] for all but the fi rst source. A flowed multilevel inverter through k number of DC foundations or num ber of H bridge cells will provide (2k+1) levels to synthesize the AC output wavefor m.

These incomes that for a five-level inverter (FLI), two DC sources and two cascaded H-bridge cells are required [5], [10]. Where a multicarrier PWM technique is accepted for obtaining the cascade inverter switching signals, n−1 carriers through same carrier frequency fc, and same peak to peak amplitude AC, are also compulsory. For the five-level decanted inverter in [1] for example, the additional H-bridge inverter, DC source, and development in the number of carriers all add to upsurge in components count and costs that will finally lead to increase in swapping losses and system size. Several attempts have been made in the recent past by sleuths to synthesize the multilevel inverter (MLI) through few number of H-bridge cells, avoiding the (2k + 1) levels theory. Even when high level MLI is to be industrialized

from few number of H bridge cells, a quite number of supplementary switches and di odes are usually incorporated in the power circuit resulting in additional control circu it designs for cells were organized for an eleven level cascaded H bridge MLI, extra four switches and eight diodes were combined to realize the design objective no effor t was made topresent the control circuit and its process of design which is predicted t o be complex. Inall the FLIs industrialized using a single H bridge cell there are the presence of one or more extra switches and diodes finished extra control circuits. For instance, in some schemes two auxiliary switches through two anti bidirectional dio des, two other diodes through which the capacitors are discharged and two DC voltag e sources have been deployed in addition to the single k cell structure [10], [16].

In other schemes, one auxiliary switch, four diodes and either two DC sources or two capacitors across a boost converter have in addition to the single k cell been intended to realize the FLIs output voltages [12], [14], [18]. Outstanding to the compl exity of the control circuit structures for the five level inverters, few authors available the control scheme while several others made little or no effort to deliberate the proc edures of the control circuit designs. In all, the sympathies of the five level inverters were all power circuit based. The compulsory levels of harmonics reduction knowled geable the different choices of the controller circuit designs by the writers. It is quite anticipated that if the realization of the FLI is control circuit based exploiting the soli tary H bridge cell disadvantaged of auxiliary power mechanisms rather than power ci rcuit based using the single H bridge cell with extra power circuit mechanisms, the s ubsequent inverter will be smaller, lighter, andsimpler, implying greater dependability lower cost plus control protection.

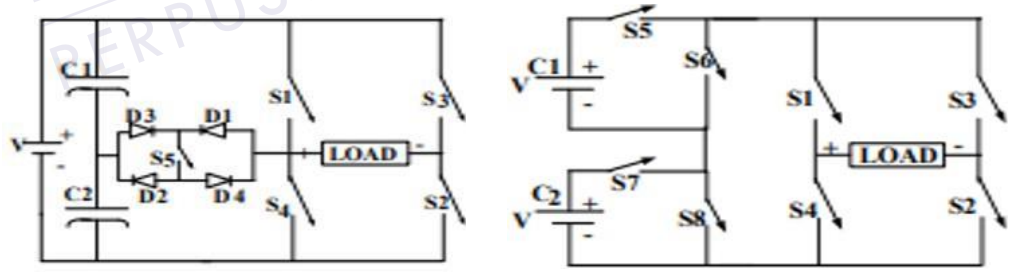
A control circuit based novel five level inverter using digital counter in the ge neration of switching signals for a single phase inverter has been proposed [1] to circ umvent further addition of power switches to the conventional H bridge invertercell when compared to the attempts made by recent researchers to achieve similar results using the H bridge cell but with additional auxiliary power switches as has been x ra yed above. A single phase H bridge five level inverter topology The circuit consists o f four switching devices S1, S2, S3, and S4, with two devices each in one

leg of the two leg inverter. The inverter uses a pair of complimentary controlled swit chesin each inverter leg, i.e. (S1, S2) and (S3, S4).

The two switches in each leg operate in a complimentary pair to avoid short c ircuiting ofthe dc source. The FLI output is a staircase waveform derived from the co nventional single phase modified sine wave inverter having α as angle of zero voltag e between the positive and negative half cycles of the inverter output. Generally, the number of switching angles in a quarter cycle of a staircase voltage waveform is limi ted to s. The numberof harmonics, consequently, that can be removed in the wavefor m is incomplete to s − 1.For the FLI output voltage waveform, only twoswitching an gles are there in a quarter of a cycle which interprets to the fact that only one harmo nics can be removed.

A. Type A Topology

In Type A there exist two sections namely Level selection part and Polarity Reversal part [1]. Level selection can be done by an Auxiliary bidirectional switch and a 4- switch Bridge takes care of polarity reversal enabling bipolar voltage levels. The basic five level Topology is shown in Figure 2.2 (a) and (b).

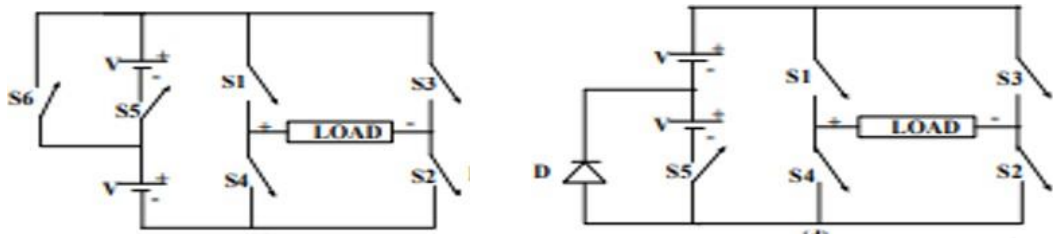


(a) (b)

Figure 2. 2 (a), (b): Type A Topology [1].

B. Type B Topology

The Level selection in Type B contains switches only and/or Diodes and Polarity Re versal part [2, 4]. The Level selection can be done by only four bidirectional switche s and a 4switch Bridge takes care of polarity reversal enabling bipolar voltage levels as depictedin Figure 2.3 (c) and (d).

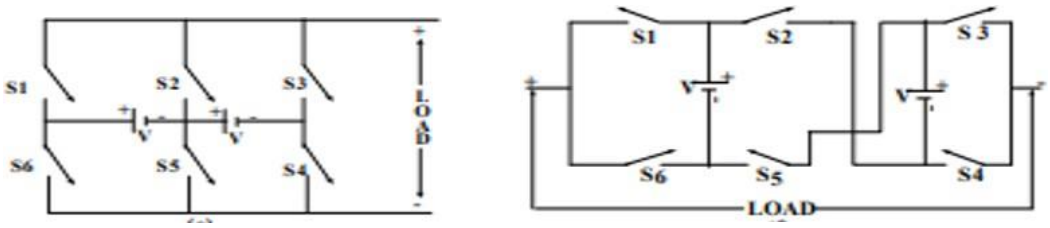


(c) (d)

Figure 2. 3 (c), (d): Type B Topology [1].

C. Type C topology

The Type C is formed by back to back connection of two H bridges [3][5], which ha s three leg structure with six unidirectional as depicted in Figure 2.4 (e). In the literat ure same three leg topology is depicted in Figure 2.4 (f) as cross connected structure and in Asymmetrical case this topology synthesizes seven levels with middleleg requi ring bidirectional natured.



(e) (f)

Figure 2. 4 (e), (f): Type C Topology [1].

D. Cascaded H-Bridge multilevel inverter

The cascaded H bridge multilevel inverter single phase five level as shown in Figure 2.5.In conventional multilevel inverters cascaded H bridge is best topology due to its inherent advantages for medium voltage and high power applications.

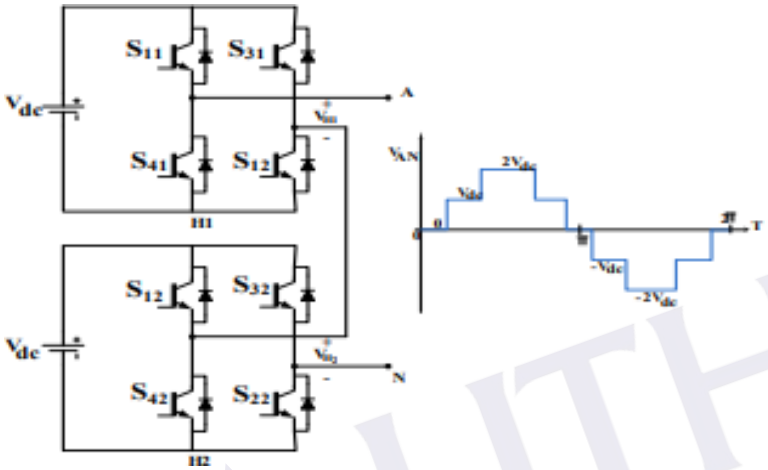


Figure 2. 5 Cascade H-Bridge inverter [3]-[5].

E. Comparison of the Various Topologies Mentioned Above

Cascade H Bridge is compared with various recent topologies. A comparative analysi s has been done as shown in Figure 2.6 keeping in the view of minimizing number o f switching devices for synthesizing five level output waveform. The analysis isfurthe r generalized for N levels as shown in Figure 2.6. The topology shown in Figure 2.3 (d) is adopted for implementation for further analysis.

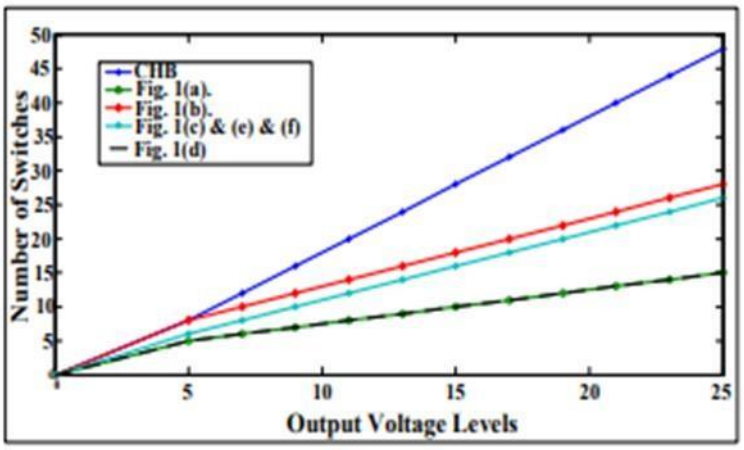


Figure 2. 6 Comparison of Various Topologies [1]

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2.4 Summary of Multilevel Inverter

The table below shows the summary of multiple papers related to multilevel inverters The summary will cover as well the result each paper produced.

Table 2.1: Summary of Multilevel Inverter

Year	Reference	Tittle	Summary
2014	[30]	Power quality improvement of DC-AC converter by using Cascaded H-Bridge Multilevel Inverter	➢ This paper present different levels of inverter with multiple type of strategies control (pulse width modulation carrier based). One of the feature of CHB-MLI is been able to integrate resources from renewable energy such as wind energy, fuel sell, solar etc., to the grid without a transformer. ➢ Among all the techniques at 7 - level CHB-MLI,PD technique is found to be the lowest THD with 23.85% compared to

Table 2.1: (continue)

			POD 27.4% and APOD 37.13% respectively.
2015	[31]	Analysis of Cascaded Multilevel inverters for Active Harmonic Filtering in Distribution Network	➢ This research paper provides the analysis of multilevel inverter involved with the active power filter with different condition of supply. The multilevel inverters proposed in this paper are 3- level, 5-level, 7-level, and 9-level which compensate with the filter. ➢ As simulation is performed, the harmonic present in multilevel inverter is decreased as the number of level is increased. ➢ The performance of multilevel m-level THD at 3-level, 5-level, 7-level, and 9-level are 3.48%, 2.08%, 1.82%, and 1.52% Respectively.
2016	[32]	Comparison of Harmonic and THD suppression with three and 5 level multilevel inverter-Cascaded H-Bridge	➢ This journal carried out the study of Total Harmonic Distortion (THD) and Harmonics in multilevel inverter. ➢ AS the simulation was performed in Matlab/Simulink with three level and five level Cascaded Multilevel Inverter compared

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